Notice of Allowability	Application No.	Applicant(s)	
	09/991,628	SAULSBURY, ASHLEY	
	Examiner	Art Unit	
	Chuong D. Ngo	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *papers filed on 12/22/2004*.

2. ☒ The allowed claim(s) is/are *1-10,12,13,15-19,21 and 23*.

3. ☒ The drawings filed on *21 November 2001* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Chuong D Ngo
Primary Examiner
Art Unit: 2193

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Applicant's representative, Thomas D. Franklin on 05/05/2005.

The application has been amended as follows:

Amendments to the Claims:

This listing of claims proposed by applicant have replaced all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Previously Presented) A processing core that executes a parallel multiply accumulate operation, the processing core comprising:

a first input operand register comprising a plurality of first input operands;

a second input operand register comprising a plurality of second input operands;

a third input operand register comprising a plurality of third input operands;

a plurality of functional blocks that each perform a multiply accumulate operation, wherein an instruction for the multiply accumulate operation indicates a rounding algorithm to use, and the rounding algorithm is one of a plurality that can be indicated by various multiply accumulate instructions;

an output operand register comprising a plurality of output operands, wherein each of the plurality of output operands is related to one of the plurality of first input operands, one of the plurality of second input operands and one of the plurality of third input operands.

2. (Previously Presented) The processing core as set forth in claim 1, wherein:

each of the plurality of functional blocks produce a result equal to multiplying the first input operand with the second input operand to produce a product and adding or subtracting the third input operand to that product, and

the instruction specifies whether an addition or a subtraction is performed.

3. (Original) The processing core as set forth in claim 2, wherein the product is truncated before adding the product to the third input operand.

4. (Original) The processing core as set forth in claim 2, wherein the product is rounded before adding the product to the third input operand.

5. (Original) The processing core as set forth in claim 1, wherein a very long instruction word includes a plurality of parallel multiply accumulate operations.

6. (Original) The processing core as set forth in claim 1, wherein the first through third input operands are at least one of following formats: integer, floating-point, fixed-point, and two's complement.

7. (Original) The processing core as set forth in claim 1, wherein the first through third input operands are at least one of: 128 bit values, 64 bit values, 32 bit values, 16 bit values, and 8 bit values.

8. (Currently Amended) A method for determining a plurality of output operands, the method comprising:

loading a multiply accumulate instruction;

decoding the multiply accumulate instruction **wherein the multiply accumulate instruction specifies one of a plurality of rounding algorithms**;

loading a plurality of multiplicands, a plurality of multipliers and a plurality of accumulate values;

processing a first multiplicand, a first multiplier and a first accumulated value in order to produce a first output operand;

processing a second multiplicand, a second multiplier and a second accumulated value in order to produce a second output operand;

~~**determining if the first output operand is larger than a predetermined value;**~~

~~**replacing the first output operand with a predetermined constant;**~~ and

storing the first output operand and second output operand.

9. (Original) The method of claim 8, further comprising:

loading a second multiply accumulate instruction;

decoding the second multiply accumulate instruction;

loading a second plurality of multiplicands, a second plurality of multipliers and a second plurality of accumulate values;

processing a third multiplicand, a third multiplier and a third accumulated value in order to produce a third output operand;

processing a fourth multiplicand, a fourth multiplier and a fourth accumulated value in order to produce a fourth output operand;

storing the third output operand and fourth output operand; and

concatenating the two of the first through fourth output operands together to form a larger output operand.

10. (Original) The method of claim 8, wherein the multiply accumulate instruction and the second multiply accumulate instruction are included in the same very long instruction word (VLIW).

11. (Canceled)

12. (Previously Presented) The method of claim 8, wherein the predetermined value is equal to a largest or smallest value for the first and second output operand.

13. (Previously Presented) A method for determining a plurality of output operands, the method comprising:

loading a multiply accumulate instruction;

decoding the multiply accumulate instruction;

loading a plurality of multiplicands, a plurality of multipliers and a plurality of accumulate values;

determining a first result equal to a product of a first multiplicand and a first multiplier plus a first accumulate value;

storing the first result;

loading a second multiply accumulate instruction;

decoding the second multiply accumulate instruction;

loading a second plurality of multiplicands, a second plurality of multipliers and a second plurality of accumulate values;

determining a second result equal to a product of a second multiplicand and a second multiplier plus a second accumulate value;

storing the second result; and

arranging the first result and second result into an unified result occupying more bits than either the first or second results.

14. (Canceled)

15. (Original) The method of claim 13, wherein the multiply accumulate instruction and the second multiply accumulate instruction are included in the same very long instruction word (VLIW).

16. (Previously Presented) The method of claim 13, further comprising:

determining a second result equal to a product of a second multiplicand and a second multiplier plus or minus a second accumulate value; and

storing the second result.

17. (Original) The method of claim 13, further comprising:

determining if the first result is larger than a predetermined value; and

replacing the first result with a predetermined constant.

18. (Original) The method of claim 17, wherein the predetermined value is equal to a largest or smallest value for the first and second output operand.

19. (Previously Presented) The processing core as set forth in claim 1, wherein:

the plurality of first input operands each has a first bit length equal to a second bit length of each of the plurality of output operands, and

the instruction specifies if the plurality of output operands will be the high order bits of the result or the low order bits of the result.

20. (Canceled)

21. (Previously Presented) The method of claim 8, wherein a first rounding algorithm can be specified by the multiply accumulate instruction that causes truncation of an intermediate product, and a second rounding algorithm can be specified by the multiply accumulate instruction causes rounding of the intermediate product.

22. (Previously Presented) The method of claim 13, wherein the multiply accumulate instruction specifies one of a plurality of rounding algorithms.

23. (New) The method of claim 8, further comprising steps of:

determining if the first output operand is larger than a predetermined value; and

replacing the first output operand with a predetermined constant.

The following is an examiner's statement of reasons for allowance:

The prior art of record does not teach or fairly suggest a parallel multiply accumulate operation as recited in claims 1 and 8, wherein the multiply accumulate instruction specifies one of a plurality of rounding algorithms; or a method including processing a first and second multiply accumulate instruction to determine a first and second result, respectively, according to those steps recited in claim 8, wherein the first and second results are arranged into an unified result.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong D. Ngo whose telephone number is (571) 272-3731. The examiner can normally be reached on Tuesday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chuong D Ngo
Primary Examiner
Art Unit 2193

05/05/2005